IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants: Thomas W. Williams et al.

Assignee: Synopsys, Inc.

Title: INTELLIGENT TEST VECTOR FORMATTING TO REDUCE TEST VECTOR SIZE AND ALLOW ENCRYPTION THEREOF FOR INTEGRATED CIRCUIT TESTING

Serial No.: 09/728,022 File Date: November 30, 2000

Examiner: John J. Tabone Jr. Art Unit: 2138

Docket No.: SYN-0174

Date: December 8, 2006

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF (RESUBMITTED)

Sir:

This Appeal Brief is in support of the Notice of Appeal dated December 7, 2005. This Appeal Brief (Resubmitted)(V2) is in response to the Notification of Non-Compliant Appeal Brief dated November 27, 2006.

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INDEX

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Synopsys Inc., pursuant to the Assignment recorded in the U.S. Patent and Trademark Office on November 30, 2000 on Reel 011342, Frame 0439.

II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no other appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

III. STATUS OF CLAIMS

Claims 7-13 and 17-20 (listed in Appendix A) are pending. Claims 7-13 and 17-20 stand rejected. In the present paper, rejected Claims 7-13 and 17-20 are appealed.

IV. STATUS OF AMENDMENTS

All claim amendments in this application have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

As taught by Appellants in the Specification, page 6, line 2 to page 7, line 11:

> [T]he present invention provides a testing solution that reduces the overall cost of testing which includes costs associated with the tester and costs associated with the test circuitry on silicon. With the ability to implement millions of gates on a chip, the incremental cost of Design for Test (DFT) is relatively small. The present invention leverages the relatively inexpensive silicon to reduce the cost of the testers by moving some of the tester functionality onto the DUT itself but, unlike BIST, maintain use of deterministic test data. The present invention advantageously reduces the memory required to store fully specified test patterns.
>
> A method and circuit are described herein for testing an integrated circuit device using intelligent test vector formatting that reduces the memory required to store test patterns and also provides an encryption vehicle for the test patterns. The novel circuit includes a first memory that stores a test vector mask. The test vector mask is a sequence of bits that indicates if corresponding test vector data is deterministic or random. The test vector data used by the present invention contains a portion that is deterministically generated by automatic test pattern generation (ATPG) software and a portion that is random. A first data value of the mask indicates deterministic data and a second data value of the mask indicates random data. A second memory contains a sequence of bits that represent the deterministic test vector data. The first and second memory could be separate locations of the same memory device. Alternative variations of this method prefix the positions of deterministic data and random data such that the mask information is minimized to represent the encoded positions.
>
> A random number generator (e.g., linear feed-back shift register, LFSR) is also provided that generates a reproducible sequence of pseudo random bits that is based on a seed value. With respect to encryption, the seed value can be viewed as a key that is required for

> proper generation of the test vectors. A selector circuit, e.g., a multiplexer, is used to select bits either from the second memory or from the random number generator. The selection is based on the value of a corresponding bit of the mask vector which is coupled to the select input of the selector. The output of the selector provides a fully specified test vector for application to the integrated circuit device under test (DUT). In one embodiment, … the random number generator can be fabricated on the DUT.

Referring to FIG. 3 (shown below for convenience) and as taught by Appellants in the Specification, page 20, lines 4-13:

> The system of FIG. 3 acts to reduce the throughput of the data flowing from the tester 14′ to the DUT 16′. The embodiment of FIG. 3 reduces the tester throughput to the DUT 16′ by incorporating the LFSR circuit 230 on the DUT 16′ itself. A configurability mechanism for sending data from the tester 14′ or the compressed data source on the DUT 16′ can be built-in. The control of the source of test data to the design would lie in the hands of the control logic 250 of the tester 14′. The embodiment of FIG. 3 also offers an increase in performance. Specifically, this configuration allows for the possibility of obtaining and applying the data portion that is generated on the DUT 16′ at a faster rate than that could be achieved from a low cost tester.

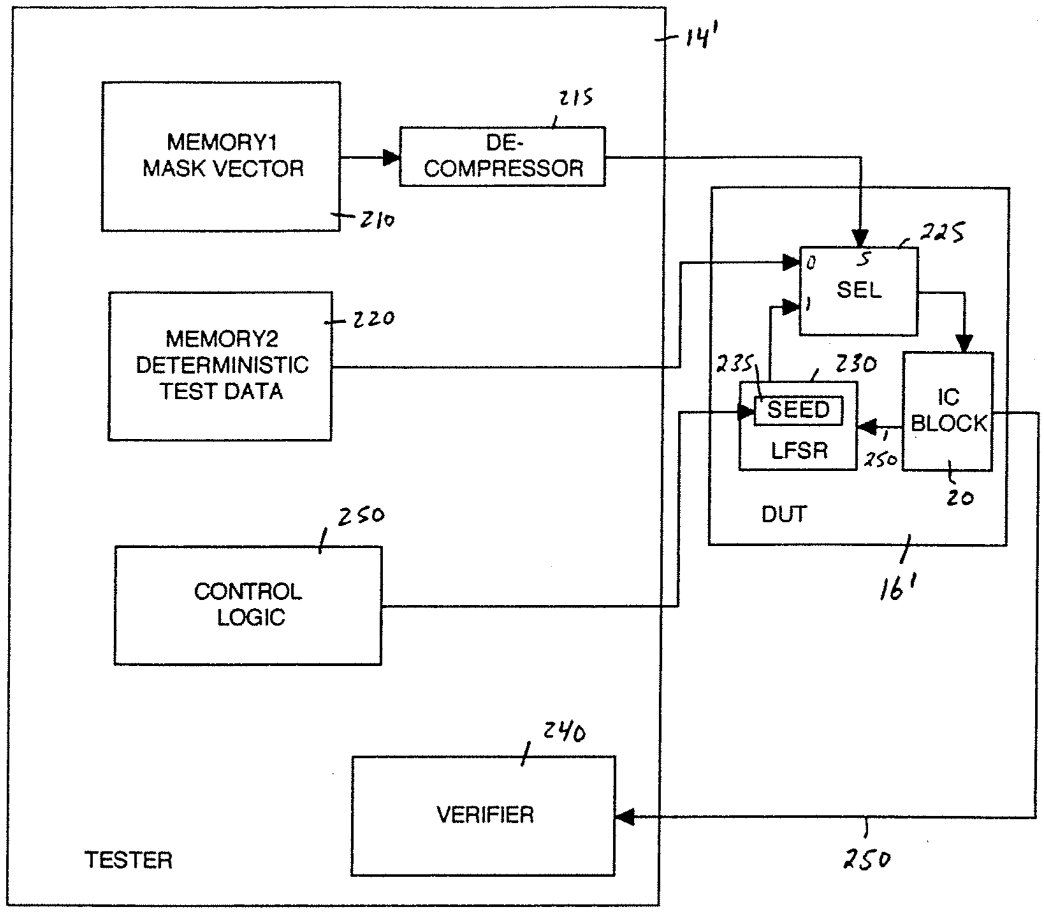


FIG. 3

Referring to FIG. 4B (shown below for convenience) and as taught by Appellants in the Specification, page 22, lines 4-16:

> FIG. 4B illustrates another embodiment of the LFSR circuit 230b which can interleave output values from the DUT 16 using OR gates 320-322. By interleaving the output values (e.g., over output lines 330-332) into the LFSR 230b, the effective "randomness" of the result is increased. This also increases error detection because an error on the output lines 330-332 will generate an improper input test pattern which will likely

lead to another departure from the expected result on the output, etc. This increases the likelihood that the error is detected by the verification circuitry 240 (FIG. 2, FIG. 3). The output lines 330-332 originate from the output of the DUT 16. The value of line 330 is ORed into the output of the first stage 310. The value of line 331 is ORed into the output of the second stage 311. The value of line 332 is ORed into the output of the third stage 312. It is appreciated that any number of stages can be used in accordance with this embodiment of the present invention.

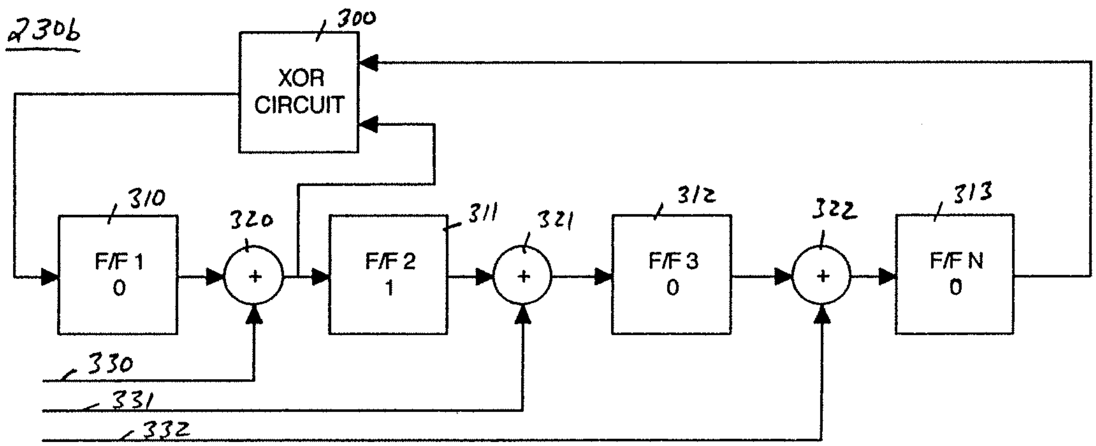


FIG. 4B

A concise explanation of the subject matter defined in each of Claims 7 and 17, referring to the Specification by page and line number and to the drawings, if applicable, follows below.

Claim 7: An integrated circuit testing system comprising: (see e.g. Specification, page 20, line 4 to page 21, line 5)

an integrated circuit tester (see e.g. FIG. 3, tester 14') comprising:

a first memory for storing therein a mask vector for characterizing corresponding test vector data (see e.g. FIG. 3, memory1 (mask vector) 210), said mask vector comprising a

plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random (see e.g. Specification, page 15, lines 17-23);

a second memory for storing therein deterministic test vector data (see e.g. FIG. 3, memory2 (deterministic test data) 220), said first and second memory coupled to a port (see e.g. Specification, page 16, lines 17-18 and page 17, lines 8-9);

an integrated circuit device under test (DUT) (see e.g. DUT 16') comprising:

a circuit block to be tested (see e.g. FIG. 3, IC block 20);

a random number generator for generating a reproducible sequence of pseudo random bits based on a seed number (see e.g. FIG. 3, LFSR 230 and seed 235); and

a selector circuit coupled to said port and for generating a test vector for application to said circuit block (see e.g. FIG. 3, selector circuit 225), said selector circuit for selecting bits as between said random number generator and said second memory based on said mask vector, said selector circuit having an output coupled to said circuit block.

Claim 17: A method for testing an integrated circuit comprising the steps of: (see e.g. Specification, page 20, line 4 to page 21, line 5 and page 22, lines 4-16)

retrieving a mask vector from a first memory (see e.g. FIG. 3, memory1 (mask vector) 210), said mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said

corresponding test vector data is pseudo random (see e.g. Specification, page 15, lines 17-23);

retrieving deterministic test vector data from a second memory (see e.g. FIG. 3, memory2 (deterministic test data) 220);

initializing a random number generator with a seed number and thereafter generating a reproducible sequence of pseudo random bits based on said seed number (see e.g. FIG. 3, LFSR 230 and seed 235);

generating an output test vector for application to a circuit block of said integrated circuit, said step d) comprising the step of selecting bits as between said random number generator and said second memory based on said mask vector (see e.g. FIG. 3, selector circuit 225 and IC block 20);

applying said output test vector to said circuit block (see e.g. FIG. 3, IC block 20, memory2 (deterministic test data) 220, LFSR 230);

obtaining an output generated by said circuit block in response to said output test vector (see e.g. FIG. 3, output 250); and

supplying said output generated by said circuit block to an input of a stage of said random number generator (see e.g. FIG. 3, output 250, LFSR 230 and FIG. 4B, outputs 330, 331, 332, LFSR 230b).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following issues are presented to the Board of Appeals for decision:

(A) Whether Claims 7-10, 13, 17, 19, and 20 are patentable under 35 U.S.C. 103(a) over U.S. Patent 5,444,716 (Jarwala).

(B) Whether Claims 11, 12, and 18 are patentable under 35 U.S.C. 103(a) over Jarwala in view of U.S. Patent 6,101,622 (Lesmeister).

VII. ARGUMENTS

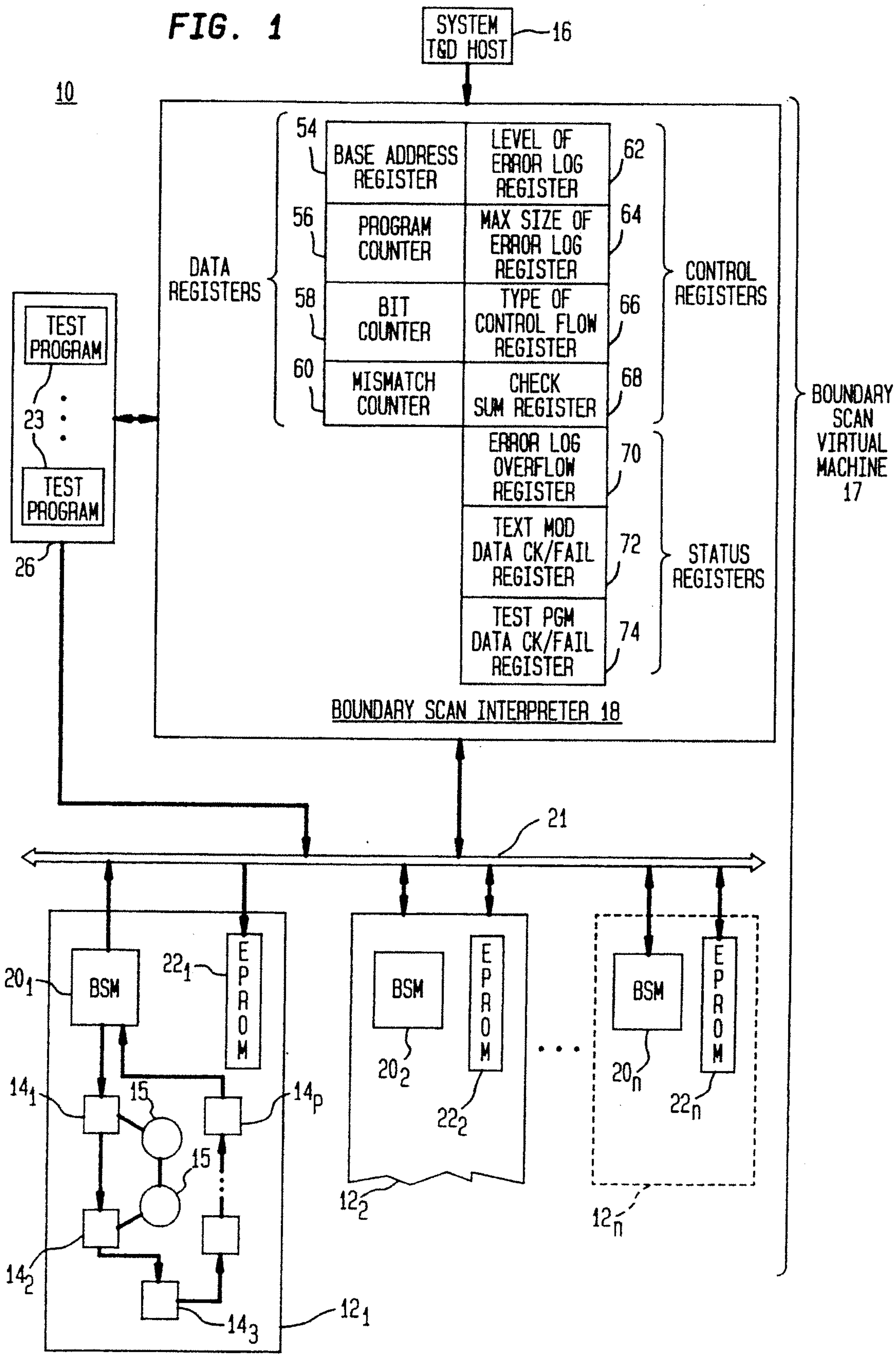
A. Claims 7-10, 13, 17, 19, and 20 are patentable under 35 U.S.C. 103(a) over U.S. Patent 5,444,716 (Jarwala).

1. Jarwala: Overview

Referring to FIG. 1 (shown below for convenience), Jarwala teaches a test system 10 that can test a plurality of circuit boards 12. Col. 2, lines 64-66. Each circuit board has a Boundary Scan architecture, wherein each Boundary Scan cell comprises a single-bit register associated with an electronic component 15, such as an integrated circuit. Col. 3, lines 1-2 and 8-11. Actual testing of circuit boards 12 is carried out by a Boundary Scan Master Virtual Machine (BVM) 17 that includes an interpreter 18 and a plurality of Boundary Scan Masters (BSM) 20, wherein each BSM 20 controls the testing of a circuit board 12. Col. 3, lines 37-45.

Test system 10 includes a system test and diagnosis host 16 that initiates testing and diagnosis without regard to the specific nature of the board 12 to be tested. Col. 2, lines 29-32. BVM 17 interprets a testing command from host 16 and communicates to each board 12 at least one command that causes board 12 to commence testing with a test program specific to that board 12. Col. 2, lines 32-38. Each BSM 20 includes a process and a set of registers for executing that test program and to provide the results of such testing to interpreter 18 (of BVM 17). Col. 2, lines 40-44. BVM 17 enables host 16 to manage testing without concern as to the specific details of the boards 12 under test.

FIG. 1



 (SN: 09/728,022)

2. Claims 7-10, 13, 17, 19, and 20 are not taught by Jarwala.

Claim 7 recites:

> An integrated circuit testing system comprising:
>
> a) an integrated circuit tester comprising:
>
> a1) a first memory for storing therein a mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random; and
>
> a2) a second memory for storing therein deterministic test vector data, said first and second memory coupled to a port;
>
> b) an integrated circuit device under test (DUT) comprising:
>
> b1) a circuit block to be tested;
>
> b2) a random number generator for generating a reproducible sequence of pseudo random bits based on a seed number; and
>
> b3) a selector circuit coupled to said port and for generating a test vector for application to said circuit block, said selector circuit for selecting bits as between said random number generator and said second memory based on said mask vector, said selector circuit having an output coupled to said circuit block.

Appellants respectfully submit that Jarwala fails to disclose or suggest the recited IC tester and IC DUT. The Office Action states that TVO memory 32, ATPG 34, and multiplexer 36 teach the recited second memory, random number generator, and selector circuit, respectively. Appellants traverse this characterization. Specifically, as recited in

Claim 7, the random number generator and the selector circuit are included on the integrated circuit device under test (IC DUT). In contrast, Jarwala teaches testing a circuit board 12, wherein each circuit board 12 includes a plurality of electrical components 15, such as ICs. Therefore, Jarwala fails to teach the recited IC DUT.

The Office Action admits that Jarwala fails to explicitly disclose the first memory that stores a mask vector. Moreover, as recited in Claim 7, the first and second memories are included on an IC tester. The Examiner ignores this limitation. Notably, the separation of components between the IC tester and the IC DUT provides significant advantages. Specifically, the recited system acts to reduce the throughput of the data flowing from the tester to the DUT and increases performance, i.e. allows for the possibility of obtaining and applying the data portion that is generated on the DUT at a faster rate than that could be achieved from a low cost tester. Specification, paragraph [0046] (see above).

Because Jarwala fails to teach the recited configuration of the IC tester and the IC DUT, Jarwala cannot achieve the tester throughput and the performance provided by Appellants' recited testing system. Because Jarwala fails to disclose or suggest the recited testing system, Appellants request reconsideration and withdrawal of the rejection of Claim 7.

Claims 8-10 and 13 depend from Claim 7 and therefore are patentable for at least the reasons presented for Claim 7. Based on those reasons, Appellants request reconsideration and withdrawal of the rejection of Claims 8-10 and 13.

Claim 17 recites:

> A method for testing an integrated circuit comprising the steps of:
>
> a) retrieving a mask vector from a first memory, said mask vector for characterizing

corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random;

b) retrieving deterministic test vector data from a second memory;

c) initializing a random number generator with a seed number and thereafter generating a reproducible sequence of pseudo random bits based on said seed number;

d) generating an output test vector for application to a circuit block of said integrated circuit, said step d) comprising the step of selecting bits as between said random number generator and said second memory based on said mask vector

e) applying said output test vector to said circuit block;

f) obtaining an output generated by said circuit block in response to said output test vector; and

g) supplying said output generated by said circuit block to an input of a stage of said random number generator.

Appellants respectfully submit that Jarwala fails to disclose or suggest the recited step of supplying the output generated by the circuit block to an input of a stage of the random number generator (i.e. step g)). The recited step, as discussed in reference to FIG. 4B, can interleave output values from the DUT into the LFSR, thereby advantageously increasing the effective randomness of the result as well as error detection capability. Specification, paragraph [0051] (see above).

The Office Action characterizes the Test Vector Manipulation register (of BSM internal registers 29) as being the recited circuit block. Appellants traverse this characterization. Specifically, the output test vector is applied to a circuit block of the integrated circuit.

Therefore, the recited circuit block cannot be taught by the Test Vector Manipulation register of Jarwala.

Because Jarwala fails to teach supplying the output generated by the circuit block to an input of a stage of the random number generator, Jarwala cannot achieve the effective randomness provided by Appellants' recited method. Because Jarwala fails to disclose or suggest the recited method, Appellants request reconsideration and withdrawal of the rejection of Claim 17.

Claims 19-20 depend from Claim 17 and therefore are patentable for at least the reasons presented for Claim 17. Based on those reasons, Appellants request reconsideration and withdrawal of the rejection of Claims 19-20.

B. Claims 11, 12, and 18 are patentable under 35 U.S.C. 103(a) over Jarwala in view of U.S. Patent 6,101,622 (Lesmeister).

1. Jarwala: Overview (see Section A)

2. Lesmeister: Overview

Lesmeister teaches an asynchronous IC tester that includes a set of channels interconnected by a runtime bus, thereby allowing the channels to communicate with one another during a test. Col. 2, lines 16-19. Each channel accesses a separate terminal of a DUT and, during each cycle of the test, each channel may transmit a test signal to the DUT, sample a DUT output signal, and/or compare stored sample data. Col. 2, lines 19-24. Data stored in each channel can be compressed into a set of one or more vectors. Col. 4, lines 45-58.

3. Claims 11, 12 and 18 are not taught by Jarwala and Lesmeister.

Claims 11 and 12 depend from Claim 7 and therefore are patentable for at least the reasons presented for Claim 7. Notably, Lesmeister fails to remedy the deficiencies of Jarwala with respect to Claim 7. Because Jarwala and Lesmeister fail to disclose or suggest the limitations of Claim 7, these references must logically also fail to disclose or suggest dependent Claims 11 and 12. Therefore, Appellants request reconsideration and withdrawal of the rejection of Claim 11 and 12.

Claim 18 depends from Claim 17 and therefore is patentable for at least the reasons presented for Claim 17. Notably, Lesmeister fails to remedy the deficiencies of Jarwala with respect to Claim 17. Because Jarwala and Lesmeister fail to disclose or suggest the limitations of Claim 17, these references must logically also fail to disclose or suggest dependent Claim 18. Therefore, Appellants request reconsideration and withdrawal of the rejection of Claim 18.

C. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejections of Claims 7-13 and 17-20 are erroneous, and reversal of these rejections is respectfully requested.

Respectfully submitted,

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VIII. APPENDIX A

1-6. (Cancelled)

7. (Previously Presented) An integrated circuit testing system comprising:

a) an integrated circuit tester comprising:

a1) a first memory for storing therein a mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random; and

a2) a second memory for storing therein deterministic test vector data, said first and second memory coupled to a port;

b) an integrated circuit device under test (DUT) comprising:

b1) a circuit block to be tested;

b2) a random number generator for generating a reproducible sequence of pseudo random bits based on a seed number; and

b3) a selector circuit coupled to said port and for generating a test vector for application to said circuit block, said selector circuit for selecting bits as between said random number generator and said second memory based on said mask vector, said selector circuit having an output coupled to said circuit block.

8. (Original) An integrated circuit testing system as described in Claim 7 wherein said selector circuit is a

multiplexer and wherein said multiplexer has a first data input coupled to said random number generator, a second data input coupled to said second memory, and a selector input coupled to said first memory, said multiplexer for passing through to said output a bit value of said first data input provided said selector input receives a first bit value and for passing through to said output a bit value of said second data input provided said selector input receives a second bit value.

9. (Original) An integrated circuit testing system as described in Claim 7 wherein said random number generator is a linear feedback shift register (LFSR).

10. (Previously Presented) An integrated circuit testing system as described in Claim 9 wherein an output of said circuit block is coupled to an input of one stage of said LFSR.

11. (Original) An integrated circuit testing system as described in Claim 7 wherein said mask vector is data compressed.

12. (Original) An integrated circuit testing system as described in Claim 11 and further comprising a decompressor coupled between said first memory and said selector circuit.

13. (Original) An integrated circuit testing system as described in Claim 7 wherein said deterministic test vector data is generated by an automatic test pattern generator (ATPG) process and downloaded into said second memory.

14-16. (Cancelled)

17. (Previously Presented) A method for testing an integrated circuit comprising the steps of:

a) retrieving a mask vector from a first memory, said mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random;

b) retrieving deterministic test vector data from a second memory;

c) initializing a random number generator with a seed number and thereafter generating a reproducible sequence of pseudo random bits based on said seed number;

d) generating an output test vector for application to a circuit block of said integrated circuit, said step d) comprising the step of selecting bits as between said random number generator and said second memory based on said mask vector;

e) applying said output test vector to said circuit block;

f) obtaining an output generated by said circuit block in response to said output test vector; and

g) supplying said output generated by said circuit block to an input of a stage of said random number generator.

18. (Previously Presented) A method as described in Claim 17 wherein said mask vector is data compressed on said first memory and wherein said step a) comprises the steps of:

a1) reading said mask data from said first memory; and

a2) decompressing said mask vector data.

19. (Previously Presented) A method as described in Claim 17 wherein said deterministic test vector data is generated by

an automatic test pattern generator (ATPG) process and downloaded into said second memory.

20. (Previously Presented) A method as described in Claim 17 wherein said steps c) and d) are performed within said integrated circuit.

IX. EVIDENCE APPENDIX

(None)

X. RELATED PROCEEDINGS APPENDIX

(None)